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Co-design of on-chip 2.5ghz rf-dc power conversion circuit for wireless sensor network node application

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ABSTRACT – This paper presents a schematic circuit of 0.18 µM CMOS rectifier designed and simulated with the 180nm Silterra process. The results of the circuit simulation show an ability to provide an output voltage of 1.6 to 1MΩ, from an input RF power of 25 microwatts (-16 dBm), with a power conversion efficiency of 67%.

1. INTRODUCTION

CMOS stands for Complementary Metal Oxide Semiconductor and it is the technology for designing rectifier on chip. CMOS rectifier is the core of integrated radio frequency energy harvesting system and its function to replenish usable DC power to microsystem applications out from incoming ambient and dedicated RF power to antenna, henceforth CMOS rectifier enables the wireless application of different microsystems such as Wireless Sensor Network (WSN), Implementable medical devices (IMD) and radio frequency identification (RFID) tag for maximal microsystem life. The radio frequency energy harvesting is a sustainable and clean energy in diverse environments as well as a potential replacement of the microsystem battery, and the performance of the CMOS rectifier is evaluated by sensitivity and power conversion efficiency (PCE). The sensitivity of rectifier is the minimum input power required to produce certain voltage, and as in previous studies [1-2] the implementation and sensitivity analyses of diode connected transistor and ultra-low power diode in different RF power conversion circuits, had resulted that radio frequency energy harvesting system solves the constraint of high power consumption, and small battery size of microsystem, and differential cross coupled rectifier was found a highly sensitive, with sensitivity of -31dBm. Definition the PCE is the percentage of the ratio of output power to input power as in equation (1),

$$PCE = \frac{P_{out}}{P_{in}} \times 100\% \qquad (1)$$

where P_{out} is the output power, and P_{in} is the input power of the RF wave. In our design, we use a cross connect topology with a 2.5 GHz operating frequency similarly to the 4G / WiMAX RF signal broadcast at 2.5 GHz in urban environments such as an office in short-distance from cell phone tower. (Yan L. and Wing, K. 2018) stated that transistor-diode connected transistor recommended to design an efficient full wave and low power rectifier circuit [3] and as a previous study [4] the CMOS cross connect rectifier is the most efficient so far. As well as a previous study [5], a 67% PCE was obtained with differential rectifier, and an efficiency of 40% was achieved at [6]. Figure 1 shows an equivalent circuit of the on-chip power conversion circuit.

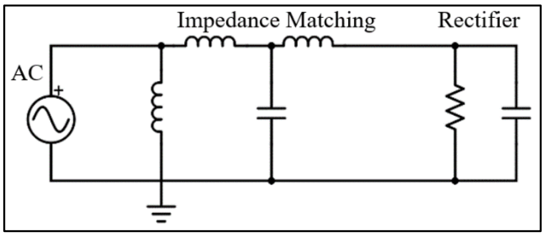

Figure 1 Equivalent circuit of rectifier with impedance matching network and AC voltage source.

2. METHODOLOGY

The specification of the CMOS rectifier circuit was determined, instances were added and wired, and the input power of the port instance was set at -16 dBm, the operating frequency at 2.5 GHz, the load at 100KΩ and after verification of the schematic design, the simulation was performed from the analog design environment with spectre simulator for an input range of -40 dBm to 10 dBm, and results were validated and recorded. The single-stage rectifier has been cascaded over three stages in series, to increase the output voltage and expand the dynamic range of power conversion efficiency. The flow chart diagram of the design of the CMOS rectifier circuit is illustrated in Figure 2.

3. RESULTS AND DISCUSSIONS

Simulation results of the output DC voltage of single stage rectifier is 0.72V, and of each stage of the 3-stage rectifier are 0.6V, 1V, and 1.6V respectively. In table one summery of simulation parameters and specification, with output DC voltage results.

The designed multistage rectifier circuit was analyzed using scattering parameter analyzes as well as periodic steady state analyses; rectifier circuit with two ports used, the results show reflection coefficient value (S11) is less than -10 dB and the simulation graph is illustrated in Figure 3, and the output DC voltage at each stage of the multistage rectifier is shown in Figure 4. In Table 2, a summary and comparison of the performance of the rectifier circuit designed in literature.

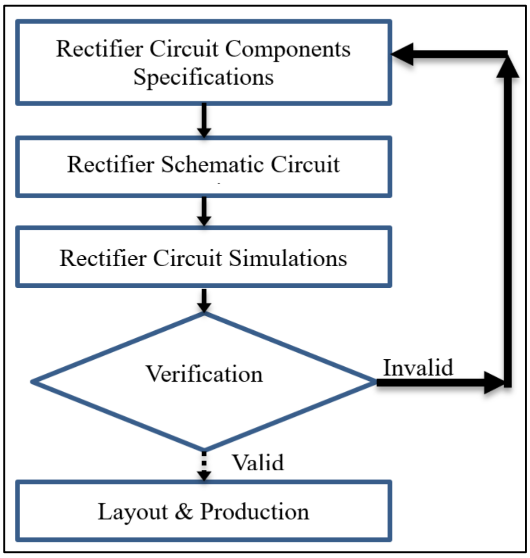

Figure 2 Flow Chart Rectifier CMOS Circuit Design.

Table 1 0.18µm CMOS Rectifier circuit simulation specification for single stage and 3-stages.

Parameter	Data (1-Stage)	Data(3-Stages)
Frequency	2.5GHz	2.5GHz
Input Power	-16dBm	-16dBm
Load (Ω)	1M	1M
Output Voltage	0.722V	1.6 V

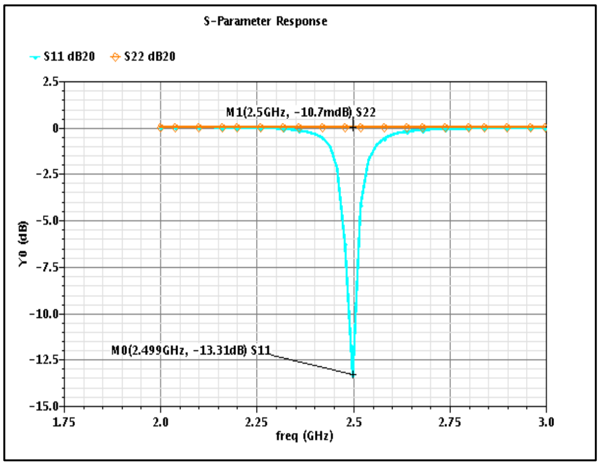

Figure 1 Reflection Coefficient (S11) at 2.5GHz.

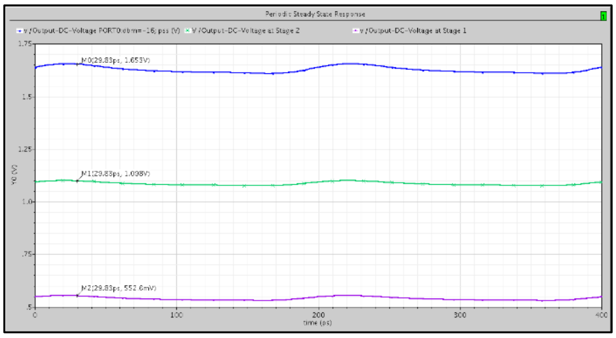

Figure 4 Output DC voltage at each stage of the rectifier.

Table 2 Summary table for comparing performance with previous work in the literature.

Specs	F (Hz)	Power (P_{in})	No of Stage	V_{out}	PCE
[5]	953 M	-12.5 dBm	1	0.6 V*	67%
[6]	868 M	-20 dBm	5	1.4 V*	40%
This Work	2.5 G	-16 dBm	3	1.6 V	67%

*value estimated from graph

4. CONCLUSION

On-Chip rectifier circuit was designed using CMOS technology with Silterra 0.18µm Process. The designed 2.5GHz differential cross connect rectifier, can produce a DC voltage of 1V from a signal of only 13 microwatts. The designed impedance matching network with a reflection coefficient of -17 dBm used to transfer all available power to the DC output voltage and improve the efficiency of the rectifier circuit.

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