Proposed reliable 16-bit pass transistor logic based full adder circuit design

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ABSTRACT – This paper presents design of 16-bit pass transistor logic based full adder. Authors have presented performance comparisons between proposed 1-bit full adder with other published adders: presented in authors' published journal [1]. The main objective of this paper is to extend proposed adder to 16-bit full adder and to validate the performance. Buffer unit; sense amplifiers are used in the proposed 16-bit adder to retain the logic computation. Comparison in term of power incremental percentage before and after implementing sense amplifiers is presented in this paper. Monte Carlo simulation has been carried out to identify the stability of this circuit; the standard deviation ranges relatively low 0.002 to 0.003. Proposed circuit is designed in layout using Microwind EDA tool in 45nm process technology.

1. INTRODUCTION

Parallel adders are extensively applied for arithmetic operations in electronics devices, microprocessors, digital signal processing, etc. [2]. Ripple carry adder, a parallel adder has the smallest area and lowest in power in many cases compared to the other parallel adder classes such as Carry Look-Ahead Adders (CLA), Carry Select Adders (CS), and Conditional Sum Adders (CSA) [2]. Researchers extended proposed 18T CMOS full adder to 4-bit and 8-bit using Ripple Carry Adder (RCA). Inverter buffers are implemented in 4-bit and 8-bit due to the performance degradation caused by glitches [3]. A 16-bit hybrid adder combination with carry-look ahead and carry-select adder architectures is designed in 0.18um CMOS technology. Worst-case delay of 876.7ps and power consumption of 787.2uW identified at temperature of 125°C. [4]. Design of 16-bit adder for wide voltage range functionality with energy effectiveness for near-threshold voltage operation has been proposed and all simulations have been carried out in 65nm process technology [5]. Proposed adder is based on double pass-transistor logic (DPL) gates and static CMOS logic gates. The 16-bit adder is designed using Carry Look Ahead (CLA) technique. Sense amplifier based pass transistor logic (SAPTL) has been proposed to retain the performance of the 16-bit adder. Proposed design brings advantage for ultra-low power applications to work in Near to Threshold Voltage (NTV) region. .

2. METHODOLOGY

Design of proposed 1-bit full adder in Figure 1 is based on the Boolean Expressions as shown in equation (1) and equation (2). Proposed 1-bit full adder is further extended to 16-bit using Ripple Carry Adder method as presented in Figure 2. Buffer units, sense amplifiers [6] are used in the 16-bit adders to retain the logic computation.

$$\mathrm{SUM} = \mathrm{A} \oplus \mathrm{B} \oplus \mathrm{C} \quad (1)$$

$$\mathrm{CARRY} = (\mathrm{B} \oplus \mathrm{C})\mathrm{A} + \mathrm{BC} \quad (2)$$

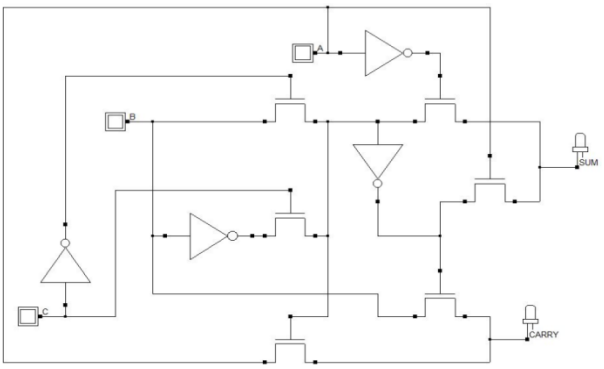

Figure 1 Proposed 1-bit full adder architecture design

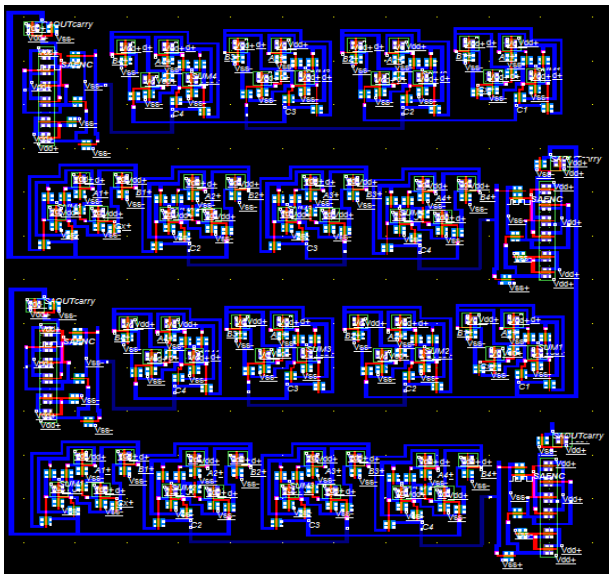

Figure 2 Proposed 16-bit full adder layout design

3. RESULT AND DISCUSSION

Table 1 shows the results of output voltages at carry and sum nodes for proposed 16-bit full adder. A buffer unit is required for every 4-bit full adder to retain the logic level. The power dissipation increases about 2% after the implementation of sense amplifiers, as shown in Figure 3. Monte Carlo runs of 5000 samples have been carried out. The lower standard deviations ranges from 0.002 to 0.003 indicate the stability of the proposed 16-bit adder cell, as shown in Figure 4.

Table 1 Output Voltage Results of Propose 16-bit full adder at Logic 111.

Adder Stage	Output Voltage Carry Node, V	Output Voltage Sum Node, V
1	0.677	0.707
2	0.536	0.656
3	0.399	0.525
4	0.308	0.321
5	0.677	0.707
6	0.536	0.656
7	0.399	0.525
8	0.308	0.321
9	0.677	0.707
10	0.536	0.656
11	0.399	0.525
12	0.308	0.321
13	0.677	0.707
14	0.536	0.656
15	0.399	0.525
16	0.308	0.321

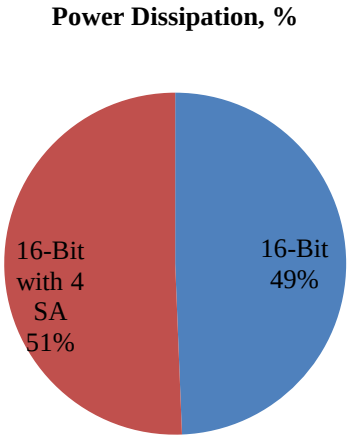

Figure 3 Power Dissipation (%)

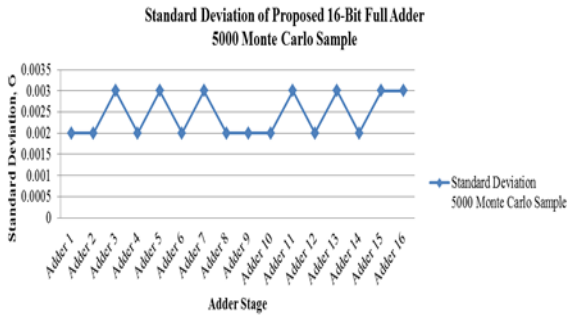

Figure 4 Standard Deviation of Monte Carlo Samples

4. CONCLUSION

Simplification of Boolean Expression to design full adder is very essential to reduce the number of transistors and inverters. Lower standard deviation of the Monte Carlo runs of 5000 samples indicates the stability and reliability of the proposed pass transistor logic based adder cell.

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